WEST Search History

Hide Items | Restore | Clear | Cancel

DATE: Monday, October 17, 2005

Hide?	Set Name	Query	Hit Count
	DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
☐	L7	L5 same (information or data)	26
☐	L6	L5 same host	4
☐	L5	L4 same interfac$4	37
☐	L4	L1 same (control$4 near5 (writ$4 or stor$4) near5 (sequen$7 or order$2))	760
☐	L3	L2 same (sequen$5 or order)	2440
☐	L2	L1 same (control$4 near5 (writ$4 or stor$4))	14657
☐	L1	(first near2 (memory or buffer or queue or storage)) same (second near2 (memory or buffer or storage or queue))	99509

END OF SEARCH HISTORY

L6: Entry 1 of 4 File: PGPB Dec 26, 2002

DOCUMENT-IDENTIFIER: US 20020199048 A1
TITLE: Enclosure for computer peripheral devices

Summary of Invention Paragraph:
[0062] U.S. Pat. No. 6,338,110 teaches a data storage system that includes a first storage channel, a first controller that is coupled to the first storage channel and a first storage device that is coupled to the first storage channel. The system also includes a second storage channel, a second storage device that is coupled to the second storage channel and a switch that is coupled to the first storage channel and the second storage channel. The switch separates the first storage channel from the second storage channel in a first state and connects the first storage channel and the second storage channel in a second state. For disk drives and RAM disks, a storage array is commonly called a disk array, in which a disk controller connects a host computer to multiple disk drives. The disk controller provides access to the actual drives in a just a bunch of drives configuration or performs striping of data across the drives in a redundant array of independent disks configuration. Storage channels include an AT Attachment, a small computer system interface, a fiber channel or storage system architecture. The external access interfaces often include industry standard architecture, bus or peripheral component-interconnect bus for host adapters, SCSI, fiber channel, or SSA. For tape drives, the storage array commonly includes individual tapes or tape silos. The controller may provide data striping capability across the tapes. The storage channels and external access interfaces are usually the same as for disk drives. For memory chip storage devices, the storage array commonly is the main processor memory, cache memory, or other memory subsystem. The controller commonly performs error detection and correction (parity and ECC) and provides data striping (usually called interleaving). The storage channels are the memory buses. The external access interfaces are commonly peripheral component-interconnect bus or processor bus. In order to maintain access to the storage devices in the event of a single controller failure (to provide high-availability), two controller cards may be attached to the same storage devices, in a dual-controller configuration. One controller may provide access to one set of storage devices and the other controller may provide access to another set of storage devices.

First Hit Previous Doc Next Doc Go to Doc#

Generate Collection Print

L7: Entry 2 of 26 File: PGPB May 26, 2005

DOCUMENT-IDENTIFIER: US 20050114575 A1
TITLE: Data transfer interface

CLAIMS:

6. The data transfer interface according to claim 5, where the controller sequentially outputs the read/write signals to the first data storage drive and the second data storage drive to initialize the first and second data storage drives for a data transfer.

Previous Doc Next Doc Go to Doc#

First Hit Previous Doc Next Doc Go to Doc#

Generate Collection Print

L7: Entry 3 of 26 File: PGPB Nov 18, 2004

DOCUMENT-IDENTIFIER: US 20040228166 A1
TITLE: Buffer chip and method for actuating one or more memory arrangements

Abstract Paragraph:
A buffer chip for actuating one or more memory arrangements, having a first data interface for receiving a data item which is to be written and for sending a data item which has been read, having a conversion unit for parallelizing the received data item and for serializing the data item which is to be sent, having a second data interface for writing the parallelized data item to the memory arrangement via a memory data bus and for receiving the data item read from the memory arrangement via the memory data bus; having a write buffer storage for buffer-storing the data item which is to be written, having a control unit in order, after reception of a data item which is to be written via the first data interface in line with a write command, to interrupt the data from being written from the write buffer storage via the second data interface upon a subsequent read command, in order to read the requested data into the buffer chip via the second data interface.

Previous Doc Next Doc Go to Doc#

First Hit Previous Doc Next Doc Go to Doc#

Generate Collection Print

L7: Entry 4 of 26 File: PGPB Jul 8, 2004

DOCUMENT-IDENTIFIER: US 20040133718 A1
TITLE: Direct access storage system with combined block interface and file interface access

CLAIMS:

1. A storage system comprising: a first interface configured to receive block-level I/O requests; a second interface configured for file-level I/O; a third interface configured for communication with another storage controller; and a data communication path suitable for data communication with physical storage in order to exchange data with the physical storage in response to the block-level I/O request and the file-level I/O requests, wherein the block-level I/O requests are serviced by exchanging data with a first storage area of the physical storage and the file-level I/O requests are serviced by exchanging data with a second storage area of the physical storage, wherein the first storage area is accessed as a first logical volume and the second storage area is accessed as a second logical volume, wherein the first logical volume and the second logical volume define a consistency group, wherein data contained in the first logical volume and in the second logical volume can be communicated to the other storage controller in order to replicate the data to secondary storage accessible by the other storage controller, wherein time consistency of write operations made to the first logical volume and to the second logical volume is maintained at the secondary storage.

Previous Doc Next Doc Go to Doc#

First Hit Previous Doc Next Doc Go to Doc#

Generate Collection Print

L7: Entry 5 of 26 File: PGPB Oct 2, 2003

DOCUMENT-IDENTIFIER: US 20030187569 A1
TITLE: Vehicle-mounted electronic control apparatus

Summary of Invention Paragraph:
[0013] A vehicle-mounted electronic control apparatus according to the invention includes: a microprocessor in which a program memory, an operational RAM, an interface circuit providing a connection to a first vehicle-mounted sensor group, an interface circuit providing a connection to a first electrical load group, and a serial-parallel converter for master station are bus-connected; and a common control circuit in which a serial-parallel converter for substation that is serial-connected to the serial-parallel converter for master station, an interface circuit providing a connection to a second vehicle-mounted sensor group, and an interface circuit providing a connection to a second electrical load group are bus-connected, the common control circuit being provided with first storage means, second storage means, abnormality determination means, distribution storage means, reply packet generation means, and reply packet composing means. In this vehicle-mounted electronic control apparatus, the first storage means stores in sequential order command data, address data, write data, sum check collation data received by the serial-parallel converter for substation via the serial-parallel converter for master station. The abnormality determination means monitors lack or mixing of any bit information in the data stored in the first storage means. The distribution storage means transfers the write data to a device memory of a specified address based on the stored address data and write data when the command data stored in the first storage means is a write/setting command accompanied by the write data. The reply packet generation means selects reply data based on the result determined by the abnormality determination means and the command data, combines the foregoing reply data with the address data to synthesize reply information. The reply information generated by the reply packet generation means is stored in sequential order into the second storage means, and read out on the basis of a preceding input/preceding output while evacuating a delay in replying. The reply packet composing means composes in a predetermined order plural reply information to be supplied to the serial-parallel converter for substation based on the reply information read out from the second storage means. Then the reply packet composing means generates additional data based on the latest information and adds those data to the delayed and held reply information to send back resultant reply information.

Previous Doc Next Doc Go to Doc#

First Hit Previous Doc Next Doc Go to Doc#

Generate Collection Print

L7: Entry 7 of 26 File: PGPB Mar 21, 2002

DOCUMENT-IDENTIFIER: US 20020033971 A1
TITLE: Image input device

Detail Description Paragraph:
[0024] The resolution of the black-and-white multivalue data conveyed to the resolution conversion portion 5 is lowered thereat with a reduction of data amount, and a resultant resolution converted data is transferred to the multivalue processing portion 6. At the portion 6, the converted data undergoes multivalue processings such as gamma correction, and a resultant processed data is transferred to and temporarily stored in the second storage portion 7. Interface portion 8 controls the first and second storage portions 7 and 8 in order to read out therefrom and transmit stored black-and-white binary data and multivalue black-and-white multivalue data alternately to PC 9.

Previous Doc Next Doc Go to Doc#

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#
Generate Collection Print

L7: Entry 10 of 26 File: USPT Nov 16, 2004

DOCUMENT-IDENTIFIER: US 6819334 B1
TITLE: Information processing apparatus and its display controller

CLAIMS:

9. A display controller coupled to a processing unit and a memory unit for storage of display data processed by said processing unit to deliver the display data to a display device, comprising: a bus interface receiving display data processed in said processing unit; a first rectangular buffer memory having a capacity for one line displayed on said display device with a number of burst transfer operations; a second rectangular buffer memory having the capacity for one line displayed on said display device with the number of burst transfer operations; a display image rotation engine which is coupled with said bus interface, and first and second rectangular buffer memories to sequentially transfer the display data to said first and second buffer memories and which responds to a command of predetermined timing for data update to deliver the display data stored in said buffer memory, to said display controller in read sequence of display data different from write sequence, wherein addresses of display data in the first and second buffer memories after a display rotation are determined by changing the output sequence of the display data in one of the first and the second buffer memories in relation to the input sequence of the display data in another of the first and second buffer memories.

Previous Doc Next Doc Go to Doc#

L7: Entry 13 of 26 File: USPT Feb 10, 1998

DOCUMENT-IDENTIFIER: US 5717946 A
TITLE: Data processor

Brief Summary Text (14):
In the data processor related to the present invention of the first aspect, when the instruction decoder decodes a multi-bit data string operation instruction which stores each bit, resultant from a predetermined operation which is executed successively between each bit of a first multi-data string continuously stored in a first memory area of the external memory and a second multi-bit data string continuously stored in a second memory area of the external memory, into the first or second memory area, the execution control unit performs a first control for, by setting an address for sequentially reading data from the first and second memory areas in the address register in response to the signal given from the instruction decoder, reading each of first and second multi-bit data strings stored in the first and second memory areas respectively from the external memory by the third bit width by burst transferring via the bus interface unit, and for storing the data strings in the data register, according to the address set in the address register, a second control for, by giving the signal specifying the predetermined operation to the operation unit based on the signal given from the instruction decoder, performing the predetermined operation between the first data string of the third bit width and the second data string of the third bit width having been stored in the data register in unit of the second bit width, and for storing the operation result again in the data register as a third data string of the third bit width, a third control for, by setting an address for sequentially storing data in the first or second memory area in the address register in response to the signal sent from the instruction decoder, storing the third data string of the third bit width having been stored in the data register in the first or second memory area by burst transferring via the bus interface unit, according to the address set in the address register, and a fourth control for, by repeating the first, second and third controls for predetermined times in response to the signal sent from the instruction decoder, storing the third data string successively into the first or second memory area.

Brief Summary Text (15):
In the data processor related to the present invention of the second aspect, when the instruction decoder decodes a multi-bit data string operation instruction which stores each bit, resultant from a predetermined operation which is executed successively on a multi-bit data string continuously stored in a first memory area of the external memory, into the first memory or in a second memory area other than the first memory area, the execution control unit performs a first control for, by setting an address for sequentially reading data from the first memory area in the address register in response to the signal sent from the instruction decoder, reading the multi-bit data string stored in the first memory area from the external memory by the third bit width by burst transferring via the bus interface unit, and for storing the data string in the data register, according to the address set in the address register, a second control for, by giving the signal specifying the predetermined operation to the operation unit based on the signal given from the instruction decoder, performing the predetermined operation on a first data string of the third bit width stored in the data register in unit of the second bit width, and store the operation result again as a second data string of the third bit

width, a third control for, by setting an address for sequentially storing data in the first or second memory area in the address register in response to the signal sent from the instruction decoder, storing the second data string of the third bit width having been stored in the data register in the first or second memory area by burst transferring via the bus interface unit, according to the address set in the address register, and a fourth control for, by repeating the first, second and third controls for predetermined times in response to the signal sent from the instruction decoder, and storing the second data string successively into the first or second memory area.

CLAIMS:

1. A data processor, comprising:

an external memory connected to a data bus having a first bit width;

an instruction decoder for decoding instructions;

an execution control unit for generating control signal to control the execution of the instructions by being given the signal indicating the results of instruction decoding by said instruction decoder;

an instruction execution unit which has a data register for holding the data to be processed of the instruction to be executed, an address register for holding the address of said data to be processed in said external memory and at least one operation unit for performing the operation on data of a second bit width equal to or longer than said first bit width, and which executes the instructions according to the control signal outputted from said execution control unit; and

a bus interface unit which inputs/outputs the data necessary to execute said instruction by burst transferring data having a third bit width longer than said second bit width from/to said external memory by outputting one address n times (n.gtoreq.2) to fetch the data n consecutive times;

wherein, when said instruction decoder decodes a multi-bit data string operation instruction which stores each bit, resultant from a predetermined operation which is executed successively between each bit of a first multi-data string continuously stored in a first memory area of said external memory and a second multi-bit data string continuously stored in a second memory area of said external memory, into said first or second memory area,

said execution control unit performs

a first control for, by setting an address for sequentially reading data from said first and second memory areas in said address register in response to the signal given from said instruction decoder, reading each of first and second multi-bit data strings stored in said first and second memory areas respectively from said external memory by said third bit width by burst transferring via said bus interface unit, and for storing the data strings in said data register, according to the address set in said address register,

a second control for, giving the signal specifying said predetermined operation to said operation unit based on the signal given from said instruction decoder, performing said predetermined operation between the first data string of the third bit width and the second data string of the third bit width, previously stored in said data register with said second bit width, and for storing the operation result again in said data register as a third data string of the third bit width,

a third control for, by setting an address for sequentially storing data in said first or second memory area in said address register in response to the signal sent

L7: Entry 22 of 26 File: USPT Feb 3, 1981

DOCUMENT-IDENTIFIER: US 4249248 A
TITLE: Programmable sequence controller with an arithmetic operation function

Detailed Description Text (13):
Referring now back to FIGS. 1A-B, description will be made hereinafter with an operation processing section which serves to successively read out the sequence instructions from the sequence program memory 30 and to execute the read out instructions. The operation processing section comprises a logic operation section 101 and an arithmetic operation section 102. The logic operation section 101 is composed of a microprogram memory 40, a model 3001 microprogram control unit (hereinafter called "MCU") 41 commercially available from Intel Corporation, Santa Clara, California, a pipeline register 42, a data selector 43 and an inverter 44 and in addition to these components, is provided with a flip-flop FF1, an address register 45 and a multiplexer 46 for interruption processings. On the other hand, the arithmetic operation section 102 is composed of a conventional digital microprocessor 50, a microprocessor memory 51, a first buffer register 52 and a gate G5 and is further provided with a second buffer register 53 and a flip-flop FF2 for interruption processings. The sequence controller further comprises an RQ-register 54 for storing data indicating one kind of monitoring and an interface 55 for connecting the microprocessor 50 with an external data input/output device such as a tele-typewriter TTY.